Solid-State Transformer (S2T) of Single Phase Matrix Converter

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ABSTRACT

Solid-State Transformer (S2T) also known as Power Electronic Transformer (PET) is applied in various industrial fields compared to the conventional transformer due to it flexible voltage transfer ratio, high power density, and low harmonic distortion. This paper presents the S2T of Single Phase Matrix Converter (SPMC) that acts as cyclo-converter. A 1kHz frequency was synthesized on the primary side of the transformer using Pulse Width Modulation (PWM) technique, whilst, the output converted by the SPMC that produces the 50Hz frequency. A part of AC to AC operation, the switching algorithm for safe-commutation technique is also presented to solve the commutation problem caused by the usage of inductive load. Minimization of size, losses and optimal efficiency are the advantages of this approach. The proposed model was simulated by using MATLAB/Simulink (MLS).

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1. INTRODUCTION

A transformer is a static device with different number of turns on a magnetic core which consist of a winding, or two or more coupled windings for inducing mutual coupling between circuits. The AC magnetic field created in the primary winding induces a current in the secondary winding in proportional to the number of turns. The main function of transformer is to increase the voltage (step-up) and to decrease the voltage (step-down). However, despite the excellent function of the transformer, there are some potential limitations for transformer such the transformer is quite heavy due to the size of magnet used. In additional, the conventional transformer is bulky, hence it requires large space for installation. It also used mineral oil which is not environmental friendly. The conventional transformer also faces power quality problems such as harmonic, voltage drop, and low performance under unbalanced load or in present of DC off-set which result larger losses and requires protection to prevent power quality problem [1].

Compared to the conventional transformer, the S2T is smaller in size and weight proportional to the similar input and output characteristic of the conventional transformer. Having efficiency compatible with the conventional transformer, S2T has electronic current limiting characteristics which does not require the use of input/output filters. Moreover, S2T are good in voltage regulation, and produce snubber-less operation due to four-step switching strategy and also generates minimal harmonics due to switching strategy [2]. The crucial of gaining optimum efficiency in S2T is to save cost in manufacturing as the S2T has smaller size than conventional transformers [3], [4].

Conventional S2T circuit topology uses a combination of rectifier and inverter circuit, resulting in high switching losses and produce rich of harmonics. In addition, the production cost of the conventional transformer is higher due to the large amount of electronic components used. In case of the center-tap

rectifier, the voltage drop becomes double and the efficiency is somewhat reduced. Together with the existence of high speed semiconductor devices, the harmonic contents of the output voltage is reduced significantly by switching techniques [5].

The Three-Level converter (TLC) and H-bridge topology have been proposed in [6] to improve the reliability of S2T based on Turn-Off Device. The control strategy is based on space vector modulation of TLC. However, the control strategy for this topology is too complicated. Reference [7], proposed full bridge phase-shift DC-DC converter that allow zero-voltage switching (ZVS) to solve power quality problems such as voltage fluctuation and grid side harmonics. However, some studies stated the system that operate under ZVS conditions can cause high switching losses due to hard switching mode from the operation of rectifier and inverter [8].

Other studies proposed the three stages structure; input stage, isolation stage and output stage. Each port consists of full bridge dc-link inverter (FBDCI), High Frequency Isolation Transformer (HFIT), and cyclo-converter which can work independently. FBDCI operate at zero voltage level, with adjustable pulse width, and symmetrical switching [9], [10]. Even though the primary side of half bridge converter can be reduced in term of size and the number of switches, this technique suffers from low efficiency due to the usage of conventional converter. In [11], a push-pull based AC to DC S2T has been proposed. Soft switching has been set to obtain substantial reduction in RMS transformer current to reduce transformer size, decrease current rating of switches and minimal conduction loss and DC ripple current which lead to high efficiency and power density. S2T operates in two modes depending on the time delay. The technique used does achieve the conclusion to reduce the third harmonic in the AC current, however at the end of the experiment the efficiency drops as the AC power drop. Nevertheless, the transformer has complex design where the switching control is too difficult as the both switches cannot be activated simultaneously.

Besides that, power electronic zigzag transformer has been proposed to interconnect mid-voltage distribution networks that it is constituted by a slow-response and low-precision thyristor converters, and a fast-response and high-accuracy voltage source converter. The dual-timescale control strategy has been presented to control both converter [12]. This topology has large size due to usage of many switches which resulting high cost. Since, the thyristor cannot stand high frequency; therefore, it is not compatible for high frequency applications. A modular multilevel converter (MMC) based S2T for DC distribution grid has been proposed in [13]. A hierarchical control system has been designed to simplify the control system and minimize the computation burden for MMC-based PET. The whole control system is divided to three layers by valve control layer. The first layer is the main controller, next is valve controller and lastly unit controllers. This converter has competitiveness on expense, volume and power loss. It is well-accepted that the converter is much more compact, inexpensive and efficient than MMC-based ones.

Research has been done to analyze the development of power electronic converters and switching devices advance as high frequency link system. The study shows the importance on high switching frequency and losses. Thus, in this work, a new topology of S2T proposed to eliminate the disadvantage of conventional transformer as well as can improve the operation performance, reduce the density, improve safety through galvanic isolation between DC and AC sides and reduce hysteresis losses [2], [14].

2. SINGLE-PHASE MATRIX CONVERTER

The SPMC consists of four bi-directional switches that are capable to conduct current in positive and negative directions and blocking the forward and reverse voltages [15]. The common emitter anti-parallel Integrated Gated Bi-polar Transistor (IGBT) is favored among researchers due to the capability to operate in high-speed switching and high current carrying [16]. IGBT provide suitable fast switching control for fine control, whilst diode acts as internal protection for IGBT capable of providing reverse blocking to switch module. Figure 1 shows the four combinations switches of two reverse blocking devices that are connected to form bi-directional switches in anti-parallel manner.



Figure 1. Flow chart dissertation process

999

3. COMMUTATION PROBLEM

SPMC has the capability in operating direct AC to AC conversion without the need of an energy storage element. However, for few applications, the major problem with SPMC is commutation. The problem happenes because the change in current due to switch commutation and pulse width modulation (PWM) switching resulting two damaging phenomena. Firstly, current spike will be generated in short-circuit path and secondly voltage spikes will be induced as a result of change in current direction across the inductance [17]–[19]. Both phenomena can lead to destruction due to the undue stress. Commutation problem occur when the inductive load is used in SPMC.

4. PROPOSED S2T OF SPMC

Figure 2 shows the propose S2T of SPMC connected with primary and secondary sides of single stage S2T. The uses SPMC could generate the high frequency current through SPMC 1 while SPMC 2 is used to release the current and voltage in low frequency due to the switching sequence.



Figure 2. Flow chart dissertation process

5. SWITCHING ALGORITHM

The switching algorithm for the proposed S2T was implemented based on the switching algorithm for safe commutation technique [20]. Both SPMC with different frequency as the SPMC 1 is set to 1 kHz and the SPMC 2 is set to 50 Hz. Both SPMC will use different control requirement depending on the value of frequency to obtain the desired output waveform. Figure 3 shows the circuit operation of S2T with safe-commutation strategy. Switching algorithm of safe-commutation strategy for 4 bidirectional switches from S1 to S4 'a' and 'b' will be performed in 4 modes. The following modes are as below:

- a. Mode 1: S1a and S4a will conduct the current to flow from the AC source during positive half-cycle, whilst S2b turn 'ON' for commutation purpose. (State 1)
- b. Mode 2: S1b and S4b will conduct the current to flow from the AC source during negative half cycle, whilst S3a turn 'ON' for commutation purpose. (State 2)
- c. Mode 3: S2a and S3a will conduct the current to flow from the AC source during positive half-cycle, whilst S4b turn 'ON' for commutation purpose. (State 3)
- d. Mode 4: S3b and S2b will conduct the current to flow from the AC source during negative half-cycle, whilst S1a turn 'ON' for commutation purpose. (State 4)

Tables 1 and 2 show the switching control for primary (SPMC 1) and secondary (SPMC 2) [20]. Table 3 show the circuit parameters for the proposed S2T of SPMC. Theoretically, the size of transformer can be minimized by increasing the switching frequency. The higher the switching frequency, the higher switching losses that occur every time the device is turned-ON. Consequently, these losses have a limit in choosing the practical maximum switching frequency. Research conducted in [2] has stated that switching losses can be nearly negligible for 1 kHz switching frequency.



Figure 3. States of switching operations with safe-commutation tehniques (a) State 1 (positive cycle), (b) State 2 (negative cycle), (c) State 3 (positive cycle), (d) State 4 (negative cycle)

Table 1. Switching Control at SPMC 1

			/		
Time interval	Input Cycle	Output Cycle	State	PWM Switch	Commutation Switch
1 to 20	Positive	Positive	1	S4a	S1a and S2b
		Negative	3	S2a	S3a and S4b
21 to 40	Negative	Positive	4	S3b	S1a and S2b
	-	Negative	2	S1b	S3a and S4b

Table 2. Switching Control at SPN	AC 2
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Time interval	Input Cycle	Output Cycle	State	PWM Switch	Commutation Switch
1 to 20	Positive	Positive	1	S4a	S1a and S2b
		Negative	4	S3b	S1a and S2b
21 to 40	Negative	Positive	3	S2a	S3a and S4b
		Negative	2	S1b	S3a and S4b

Parameter		Value		
Vin		100Vac, 50Hz (single phase)		
Load		Resistor = 50Ω		
Modulation Index		0.5		
Switching frequency	y, fs	1 kHz		
Output frequency	SPMC1	1 kHz		
	SPMC2	50 Hz		

6. COMPUTER SIMULATION MODEL

In this work, the MLS is used to simulate the proposed circuit to observe the behavior of the single stage S2T by using SPMC operation. As shown in Figure 1, the SPMC consist of four bi-directional switches. Figure 4 shows the top level main model of the proposed single stage S2T of SPMC. Subsystem is used to improve the large model by dividing into hierarchical set of smaller models to ease the implementation process. The subsystem model is as shown in Figure 4 to Figure 7. Figures 5 and 6 show the connection of SPMC with combination of four subsystems of bidirectional switches. Controller for switches

will be connected to Port A and B to control switching algorithm. The controller unit by using SPMC with commutation techniques is applied for operation of AC-AC converter as shown in Figure 7. Figure 7 (a) is controller unit for primary winding with 1 kHz output frequency while Figure 7 (b) is controller unit for secondary winding with 50Hz output frequency. The modulation index is represent the reference signal (straight line) and being compared with the carrier signal (triangular signal) by using "Relational Operator" block set to generate the required PWM output signal as shown in Figure 8. The phase detector function will produce positive and negative cycle and the signal will be simultaneously with PWM signal by using "product" block set to achieve the desired output PWM signal. The function of phase detector is to produce an 'on' pulse by comparing the sine wave with "compare to zero" block. Figure 9 shows two "compare to zero" block to compare the sine wave to form 'on' pulse for both positive and negative cycle. The modulation index is represented by the straight line to compare with carrier signal (triangular waveform) to generate the required PWM output signal. The "product" block set is implemented by using phase detector function to lock the signal into the positive and negative cycles.



Figure 4. Top main model of single stage S2T using SPMC



 Figure 5. SPMC topology model
 Figure 6. Bidirectional switch

Solid-State Transformer (S2T) of Single Phase Matrix Converter (Zafirah Zainuddin)



Figure 7. Controller circuit model for (a) SPMC 1; (b) SPMC 2



Figure 8. PWM Generator

Figure 9. Phase Detector circuit model

7. RESULTS AND DISCUSSION

The proposed converter is operated through simulation based on parameters in Table I and Table II. Figure below show the simulated waveform. A 100V sinusoidal input waveform at 50 Hz with resistor load of 50 Ω is used. Figure 10 shows the waveform of SPMC1, the frequency changed from 50 Hz to 1000 Hz. Since there has repetitive positive and negative output half-cycle in one input positive and negative cycle, the waveform obtained is as shown in Figure 10(c) and Figure 10(d). Figure 11 shows the waveform of SPMC2, as the frequency changed from 1000Hz to 50 Hz. Since there has repetitive positive and negative cycle, the waveform obtained is as shown in Figure 11(c) and Figure 11(d).



Figure 10. Waveform of (a) Input voltage (V_{in}); (b) Input current (I_{in}); (c) Primary voltage (V_p); (d) Primary current (I_p)

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Figure 11. Waveform of (a) Input voltage (V_{in}); (b) Input current (I_{in}); (c) Output voltage (V_o); (d) Output current (I_o)

Figure 12 shows the existence of undesirable spikes because of inductive load and need to be eliminated to avoid damaging stress on switching device. Figure 13 shows the existence spikes has successfully been eliminated by using the safe-commutation technique.



Figure 12. Simulation result of SPMC at frequency 50 Hz and $f_s = 1$ kHz for RL load of output waveform without safe-commutation; (a) Output voltage; (b) Output current



Figure 13. Simulation result of SPMC at frequency 50 Hz and $f_s = 1$ kHz for RL load of output waveform with safe-commutation; (a) Output voltage; (b) Output current

8. CONCLUSION

The implementation of SPMC for both sides of primary and secondary windings of a simulated electronic transformer has been presented. SPMC is flexible enough to operate in bidirectional power flow according to the switching algorithm. Two SPMC operations were investigated; without safe-commutation and with safe-commutation operation. A safe-commutation strategy has been applied and successfully eliminated voltage and current spikes causes by inductive load. Results for both SPMC were showed the effect of high frequency application of 1 kHz and 50 Hz output frequency. A 1 kHz switching frequency was investigated to observe the operation of S2T. In this study, high switching losses due the usage of high switching frequency can be neglected by selecting 1 kHz as switching frequency.

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